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Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S3	2	"6597656".pn.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/08/21 12:30
S4	15534	(parallel near switch\$5) and (@rlad<"20021219" or @ad<"20021219")	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/08/21 12:31
S5	1100	(parallel near switch\$5).ti. and (@rlad<"20021219" or @ad<"20021219")	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/08/21 12:31
S6	6	(parallel near switch\$5).ti. and ((ingress or input) adj (module or adapter or unit or card)) and (@rlad<"20021219" or @ad<"20021219")	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/08/21 12:33
S7	11	(parallel near switch\$5).ti. and ((ingress or input) near (module or adapter or unit or card)) and (@rlad<"20021219" or @ad<"20021219")	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/08/21 12:34
S8	43	(parallel near switch\$5).ti. and ((ingress or input) with (module or adapter or unit or card)) and (@rlad<"20021219" or @ad<"20021219")	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/08/21 12:38
S9	31	(parallel near switch\$5).ti. and ((ingress or input) with (module or adapter or unit or card)) and ((egress or output) with (module or adapter or unit or card)) and (@rlad<"20021219" or @ad<"20021219")	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/08/21 12:38

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S11	5	(parallel near switch\$5).ti. and ((ingress or input) with (module or adapter or unit or card)) and ((egress or output) with (module or adapter or unit or card)) and (priority) and (@rlad<"20021219" or @ad<"20021219")	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/08/21 12:47
S12	206	(parallel adj switch\$5) and ((ingress or input) with (module or adapter or unit or card)) and ((egress or output) with (module or adapter or unit or card)) and (priority) and (@rlad<"20021219" or @ad<"20021219")	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/08/21 12:50
S13	2	(parallel adj switch\$5) and ((ingress or input) with (module or adapter or unit or card)) and ((egress or output) with (module or adapter or unit or card)) and (priority) and (internal near (header or preamble or descriptor)) and (@rlad<"20021219" or @ad<"20021219")	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/08/21 12:57
S14	13	(parallel adj switch\$5) and ((ingress or input) with (module or adapter or unit or card)) and ((egress or output) with (module or adapter or unit or card)) and (priority) and (internal with (header or preamble or descriptor)) and (@rlad<"20021219" or @ad<"20021219")	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/08/21 15:19
S18	14	(parallel adj switch\$5) and ((ingress or input)) and ((egress or output)) and (priority) and ((time adj2 stamp) same (header or preamble or descriptor)) and (@rlad<"20021219" or @ad<"20021219")	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/08/21 15:30
S19	18	(parallel adj switch\$5) and ((ingress or input)) and ((egress or output)) and ((time adj2 stamp) same (header or preamble or descriptor)) and sequenc\$6 and (@rlad<"20021219" or @ad<"20021219")	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/08/21 15:32

Day : Tuesday
Date: 8/21/2007

Time: 11:28:05

 PALM INTRANET

Inventor Information for 10/722901

Inventor Name	City	State/Country
BLANC, ALAIN	TOURRETTES SUR LOOP	FRANCE
GLAISE, RENE	NICE	FRANCE
PORET, MICHEL	GATTIERES	FRANCE
WIND, DANIEL	DRAP	FRANCE

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 Jung, Y.C.; Un, C.K.; Ryu, S.M.; Lee, S.C.;
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- ☐ **2. An O(log/sup 2/ N) parallel algorithm for output queuing**
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 Zhihong Ye; Boroyevich, D.;
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7. **Formal verification of memory circuits by switch-level simulation**
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